

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

**THIS PAGE BLANK (USPTO)**

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number  
**WO 02/15244 A2**(51) International Patent Classification<sup>7</sup>: **H01L 21/205**195 Beethoven Avenue, Newton, MA 02168 (US). **HOYT, Judy, L.**; 32 Springfield Street, Belmont, MA 02478 (US).(21) International Application Number: **PCT/US01/41680**(74) Agents: **CONNORS, Matthew, E. et al.; Samuels, Gauthier & Stevens, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).**

(22) International Filing Date: 10 August 2001 (10.08.2001)

(25) Filing Language:

English

(81) Designated States (*national*): CA, JP, KR.

(26) Publication Language:

English

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(30) Priority Data:

60/225,666 16 August 2000 (16.08.2000) US

Published:

(71) Applicant: **CHENG, Zhi-Yuan** [US/US]; 14 Seventh Street, Cambridge, MA (US).

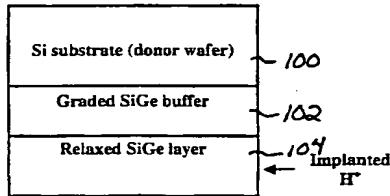
— without international search report and to be republished upon receipt of that report

(72) Inventors: **FITZGERALD, Eugene, A.**; 7 Camelot Road, Windham, NH 03087 (US). **ANTONIADIS, Dimitri, A.**;

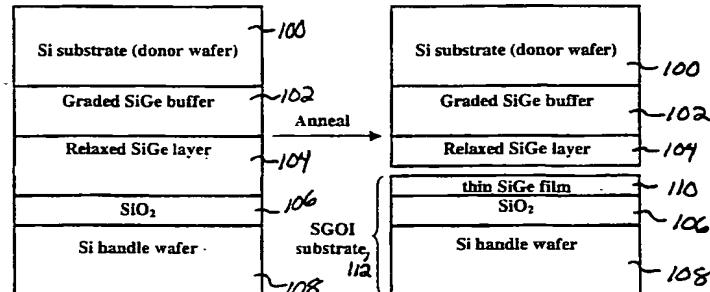
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROCESS FOR PRODUCING SEMICONDUCTOR ARTICLE USING GRADED EXPITAXIAL GROWTH

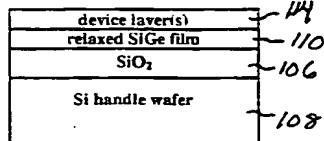
A



B



C



(57) Abstract: A process for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded  $Si_{1-x}Ge_x$  (x increases from 0 to y) is deposited on a first silicon substrate, followed by deposition of a relaxed  $Si_{1-y}Ge_y$  layer, a thin strained  $Si_{1-z}Ge_z$  layer. Hydrogen ions are then introduced into the strained  $Si_{1-z}Ge_z$  layer. The relaxed  $Si_{1-y}Ge_y$  layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, such that the second relaxed  $Si_{1-y}Ge_y$  layer remains on the second substrate. In another exemplary embodiment, a graded  $Si_{1-x}Ge_x$  is deposited on a first silicon substrate, where the Ge concentration x is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth. The relaxed GaAs layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the hydrogen ion rich layer, such that the upper portion of relaxed GaAs layer remains on the second substrate.

WO 02/15244 A2

**PROCESS FOR PRODUCING SEMICONDUCTOR ARTICLE  
USING GRADED EXPITAXIAL GROWTH**

5

**PRIORITY INFORMATION**

This application claims priority from provisional application Ser. No. 60/225,666 filed August 16, 2000.

**BACKGROUND OF THE INVENTION**

10 The present invention relates to a production of a general substrate of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ -on-insulator (SGOI) for various electronics or optoelectronics applications, and the production of monocrystalline III-V or II-VI material-on-insulator substrate.

Relaxed  $\text{Si}_{1-x}\text{Ge}_x$ -on-insulator (SGOI) is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology 15 and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc. High mobility strained-Si, strained- $\text{Si}_{1-x}\text{Ge}_x$  or strained-Ge MOS devices can be made on SGOI substrates.

Other III-V optoelectronic devices can also be integrated into the SGOI 20 substrate by matching the lattice constants of III-V materials and the relaxed  $\text{Si}_{1-x}\text{Ge}_x$ . For example a GaAs layer can be grown on  $\text{Si}_{1-x}\text{Ge}_x$ -on-insulator where x is equal or close to 1. SGOI may serve as an ultimate platform for high speed, low power electronic and optoelectronic applications.

SGOI has been fabricated by several methods in the prior art. In one method, 25 the separation by implantation of oxygen (SIMOX) technology is used to produce SGOI. High dose oxygen implant was used to bury high concentrations of oxygen in a  $\text{Si}_{1-x}\text{Ge}_x$  layer, which was then converted into a buried oxide (BOX) layer upon annealing at high temperature (for example, 1350 °C). See, for example, Mizuno et al. IEEE Electron Device Letters, Vol. 21, No. 5, pp. 230-232, 2000 and Ishilawa et al.

30 Applied Physics Letters, Vol. 75, No. 7, pp. 983-985, 1999. One of the main drawbacks is the quality of the resulting  $\text{Si}_{1-x}\text{Ge}_x$  film and BOX. In addition, Ge segregation during high temperature anneal also limits the maximum Ge composition to a low value.

U.S. Pat. Nos. 5,461,243 and 5,759,898 describe a second method, in which a 35 conventional silicon-on-insulator (SOI) substrate was used as a compliant substrate. In the

process, an initially strained  $\text{Si}_{1-x}\text{Ge}_x$  layer was deposited on a thin SOI substrate. Upon an anneal treatment, the strain was transferred to the thin silicon film underneath, resulting in relaxation of the top  $\text{Si}_{1-x}\text{Ge}_x$  film. The final structure is relaxed-SiGe/strained-Si/insulator, which is not an ideal SGOI structure. The silicon layer in the 5 structure is unnecessary, and may complicate or undermine the performance of devices built on it. For example, it may form a parasitic back channel on this strained-Si, or may confine unwanted electrons due to the band gap offset between the strained-Si and SiGe layer.

U.S. Pat. Nos. 5,906,951 and 6,059,895 describe the formation of a similar 10 SGOI structure: strained-layer(s)/relaxed-SiGe/Si/insulator structure. The structure was produced by wafer bonding and etch back process using a  $\text{P}^{++}$  layer as an etch stop. The presence of the silicon layer in the above structure may be for the purpose of facilitating Si-insulator wafer bonding, but is unnecessary for ideal SGOI substrates. Again, the silicon layer may also complicate or undermine the performance of devices 15 built on it. For example, it may form a parasitic back channel on this strained-Si, or may confine unwanted electrons due to the band gap offset between the strained-Si and SiGe layer. Moreover, the etch stop of  $\text{P}^{++}$  in the above structure is not practical when the first graded  $\text{Si}_{1-y}\text{Ge}_y$  layer described in the patents has a  $y$  value of larger than 0.2. Experiments from research shows  $\text{Si}_{1-y}\text{Ge}_y$  with  $y$  larger than 0.2 is a very good etch 20 stop for both KOH and TMAH, as described in a published PCT application WO 99/53539. Therefore, the KOH will not be able to remove the first graded  $\text{Si}_{1-y}\text{Ge}_y$  layer and the second relaxed SiGe layer as described in the patents.

Other attempts include re-crystallization of an amorphous  $\text{Si}_{1-x}\text{Ge}_x$  layer 25 deposited on the top of SOI (silicon-on-insulator) substrate, which is again not an ideal SGOI substrate and the silicon layer is unnecessary, and may complicate or undermine the performance of devices built on it. Note Yeo et al. IEEE Electron Device Letters, Vol. 21, No. 4, pp. 161-163, 2000. The relaxation of the resultant SiGe film and quality of the resulting structure are main concerns.

From the above, there is a need for a simple technique for relaxed SGOI 30 substrate production, a need for a technique for production of high quality SGOI and other III-V material-on-insulator, and a need for a technique for wide range of material transfer.

## SUMMARY OF THE INVENTION

35 According to the invention, there is provided an improved technique for production

of wide range of high quality material is provided. In particular, the production of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ -on-insulator (SGOI) substrate or relaxed III-V or II-VI material-on-insulator, such as GaAs-on-insulator, is described. High quality monocrystalline relaxed SiGe layer, relaxed Ge layer, or other relaxed III-V material layer is grown on a silicon substrate using a graded  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial growth technique. A thin film of the layer is transferred into an oxidized handle wafer by wafer bonding and wafer splitting using hydrogen ion implantation. The invention makes use of the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer structure, resulting in a simplified and improved process.

The invention also provides a method allowing a wide range of device materials to be integrated into the inexpensive silicon substrate. For example, it allows production of  $\text{Si}_{1-x}\text{Ge}_x$ -on-insulator with wide range of Ge concentration, and allows production of many III-V or II-VI materials on insulator like GaAs, AlAs, ZnSe and InGaP. The use of graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer in the invention allows high quality materials with limited dislocation defects to be produced and transferred. In one example, SGOI is produced using a SiGe structure in which a region in the graded buffer can act as a natural etch stop.

The invention provides a process and method for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded  $\text{Si}_{1-x}\text{Ge}_x$  ( $x$  increases from 0 to  $y$ ) is deposited on a first silicon substrate, followed by deposition of a relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer, a thin strained  $\text{Si}_{1-z}\text{Ge}_z$  layer and another relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer. Hydrogen ions are then introduced into the strained  $\text{Si}_z\text{Ge}_z$  layer. The relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, whereby the second relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer remains on said second substrate.

In another exemplary embodiment, a graded  $\text{Si}_{1-x}\text{Ge}_x$  is deposited on a first silicon substrate, where the Ge concentration  $x$  is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth. The relaxed GaAs layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the hydrogen ion rich layer, whereby the upper portion of relaxed GaAs layer remains on said second substrate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1C are block diagrams showing the process of producing a SGOI

substrate in accordance with the invention;

Figs. 2A and 2B are infrared transmission images of an as-bonded wafer pair and a final SGOI substrate after splitting, respectively;

Fig. 3 is a TEM cross-section view of a SiGe layer that was transferred onto the  
5 top of a buried oxide;

Fig. 4 is an AFM for a transferred SGOI substrate showing surface roughness;  
and

Figs. 5-8 are block diagrams of various exemplary embodiments semiconductor  
structures in accordance with the invention.

10

### DETAILED DESCRIPTION OF THE INVENTION

An example of a process in which SGOI is created by layer transfer is described. The experiment was performed in two stages. In the first stage, heteroepitaxial SiGe layers are formed by a graded epitaxial growth technology.

15 Starting with a 4-inch Si (100) donor wafer 100, a linearly stepwise compositionally graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer 102 is deposited with CVD, by increasing Ge concentration from zero to 25%. Then a 2.5  $\mu\text{m}$  relaxed  $\text{Si}_{0.75}\text{Ge}_{0.25}$  cap layer 104 is deposited with the final Ge composition, as shown in Fig. 1A.

The relaxed SiGe cap layer has high quality with very low dislocation defect  
20 density (less than  $1\text{E}6 / \text{cm}^2$ ), as the graded buffer accommodates the lattice mismatch between Si and relaxed SiGe. A thin layer of this high quality SiGe will be transferred into the final SGOI structure. The surface of the as-grown relaxed SiGe layer shows a high roughness around 11nm to 15nm due to the underlying strain fields generated by misfit dislocations at the graded layer interfaces and thus chemical-mechanical  
25 polishing (CMP) is used to smooth the surface. In the second stage, the donor wafer is implanted with hydrogen ion (100 keV,  $5\text{E}16 \text{H}^+/\text{cm}^2$ ) to form a buried hydrogen-rich layer. After a surface clean step in a modified RCA solution, it is bonded to an oxidized 106 Si handle wafer 108 at room temperature as shown in Fig. 1B.

The wafer bonding is one of the key steps, and the bonding energy should be  
30 strong enough in order to sustain the subsequent layer transfer in the next step. Good bonding requires a flat surface and a highly hydrophilic surface before bonding. On the other hand, the buried oxide in the final bonded structure is also required to have good electrical properties as it will influence the final device fabricated on it. In the conventional Si film transfer, thermal oxide on the donor wafer is commonly used  
35 before  $\text{H}^+$  implantation and wafer bonding, which becomes the buried oxide in the

resulting silicon-on-insulator structure.

The thermal oxide of the Si donor wafer meets all the requirements, as it has good electrical properties, has flat surface and bonds very well to the handle wafer.

Unlike the Si, however, the oxidation of SiGe film results in poor thermal oxide 5 quality, and the Ge segregation during oxidation also degrades the SiGe film.

Therefore the thermal oxide of SiGe is not suitable for the SGOI fabrication. In one exemplary experiment the SiGe film will be directly bonded to an oxidized Si handle wafer. The high quality thermal oxide in the handle wafer will become the buried oxide in the final SGOI structure.

Having a flat surface after a CMP step, the SiGe wafer went through a clean 10 step. Compared to Si, one difficulty of SiGe film is that, SiGe surface becomes rougher during the standard RCA clean, as the NH<sub>4</sub>OH in RCA1 solution etches Ge faster than Si. Rough surface will lead to weak bonding as the contact area is reduced when bonded to the handle wafer. In this exemplary embodiment, H<sub>2</sub>SO<sub>4</sub>-H<sub>2</sub>O<sub>2</sub> solution is 15 used in the place of RCA1, which also meets the clean process requirement for the subsequent furnace annealing after bonding. The SiGe surface after H<sub>2</sub>SO<sub>4</sub>-H<sub>2</sub>O<sub>2</sub> clean shows better surface roughness compared to RCA1.

After this modified clean procedure, the SiGe wafer is dipped in the diluted HF solution to remove the old native oxide. It is then rinsed in DI water thoroughly to 20 make the surface hydrophilic by forming a fresh new native oxide layer that is highly active. After spinning dry, the SiGe wafer is bonded to an oxidized handle wafer at room temperature, and then annealed at 600 °C for 3 hours. During anneal the bonded pair split into two sheets along the buried hydrogen-rich layer, and a thin relaxed Si<sub>0.75</sub>Ge<sub>0.25</sub> film 110 is transferred into the handle wafer, resulting in a SGOI substrate 25 112, as shown in Fig. 1B. A final 850 °C anneal improves the Si<sub>0.75</sub>Ge<sub>0.25</sub>/SiO<sub>2</sub> bond. Thereafter, device layers 114 can be processed on the SGOI substrate 112 as shown in Fig. 1C.

Figs. 2A and 2B are infrared transmission images of the as-bonded wafer pair and the final SGOI substrate after splitting, respectively. To investigate the surface of 30 the as-transferred SGOI substrate, transmission electron microscopy (TEM) and atomic force microscopy (AFM) were used. The TEM cross-section view in Fig. 3 shows a ~640 nm SiGe layer was transferred onto the top of a 550 nm buried oxide (BOX). Surface damage is also shown clearly at the splitting surface with a damage depth of ~100 nm.

Fig. 4 shows a surface roughness of 11.3 nm in an area of 5x5 μm<sup>2</sup> by AFM for the 35

as-transferred SGOI. The data is similar to those from as-transferred silicon film by smart-cut process, and suggests that a top layer of about 100 nm should be removed by a final CMP step.

After SiGe film transferring, only a thin relaxed SiGe film is removed and the donor wafer can be used again for a donor wafer. Starting from this general SGOI substrate, various device structures can be realized by growing one or more device layers on the top, as shown in Fig. 2C. Electrical evaluation is in progress by growing a strain Si layer on the top of this SGOI substrate followed by fabrication of strained Si channel devices.

Bond strength is important to the process of the invention. AFM measurements were conducted to investigate the SiGe film surface roughness before bonding under different conditions. One experiment is designed to investigate how long the SiGe surface should be polished to have smooth surface and good bond strength, since the surface of the as-grown relaxed SiGe layer has a high roughness around 11nm to 15nm.

Several identical 4-inch Si wafers with relaxed  $\text{Si}_{0.75}\text{Ge}_{0.25}$  films were CMPed with optimized polishing conditions for different times. Using AFM, the measured surface mircoroughness RMS at an area of  $10\mu\text{m} \times 10\mu\text{m}$  is 5.5Å, 4.5Å and 3.8Å, for wafer CMPed for 2 min., 4 min. and 6 min. respectively. After bonding to identical handle wafers, the tested bond strength increases with decreasing RMS. A CMP time of 6 min. is necessary for good strength.

In another experiment, two identical 4-inch Si wafers with relaxed  $\text{Si}_{0.75}\text{Ge}_{0.25}$  films were CMPed for 8 min. After two cleaning steps in  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  solution and one step in diluted HF solution, one wafer was put in a new  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  (3:1) solution and another in a new  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:1:5), i.e. the conventional RCA1 solution, both for 15 min. The resultant wafers were tested using AFM. The wafer after  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  solution shows a surface roughness RMS of 2Å at an area of  $1\mu\text{m} \times 1\mu\text{m}$ , which after  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  shows 4.4Å. Clearly, the conventional RCA clean roughens the SiGe surface significantly, and  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  should be used for SiGe clean.

In yet another experiment, the clean procedure is optimized before bonding. For direct SiGe wafer to oxidized handle wafer bonding (SiGe-oxide bonding), several different clean procedures were tested. It has been found that the  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  (2~4:1) solution followed by DI water rinse and spin dry gives good bond strength. Alternatively, one can also deposit an oxide layer on the SiGe wafer and then CMP the oxide layer. In this case, SiGe/oxide is bonded to an oxidized handle wafer, i.e. oxide-oxide bonding.

Among different clean procedures, it was found that  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  clean and DI

water rinse following by diluted HF, DI water rinse and spin dry gives very good bond strength.

Fig. 5 is a block diagram of an exemplary embodiment of a semiconductor structure 500 in accordance with the invention. A graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 504 is grown on a silicon substrate 502, where the Ge concentration x is increased from zero to a value y in a stepwise manner, and y has a selected value between 0 and 1. A second relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer 506 is then deposited, and hydrogen ions are implanted into this layer with a selected depth by adjusting implantation energy, forming a buried hydrogen-rich layer 508. The wafer is cleaned and bonded to an oxidized handle wafer 510. An anneal treatment at 500~600°C splits the bonded pair at the hydrogen-rich layer 508. As a result, the upper portion of the relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer 506 remains on the oxidized handle wafer, forming a SGOI substrate. The above description also includes production of Ge-on-insulator where y = 1.

During the wafer clean step prior to bonding, the standard RCA clean for the silicon surface is modified. Since the  $\text{NH}_4\text{OH}$  in standard RCA1 solution etches Ge faster than Si, the SiGe surface will become rough, leading to a weak bond. A  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  solution is used in the place of RCA1, which also meets the clean process requirement for the subsequent furnace annealing after bonding. The SiGe surface after the  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  clean showed better surface roughness compared to RCA1. After the modified RCA clean, the wafers are then immersed in another fresh  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  solution for 10 to 20 min.  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$  renders the SiGe surface hydrophilic. After a rinse in DI wafer and spin drying, the SiGe wafer is bonded to an oxidized handle wafer at room temperature immediately, and then annealed at 500~600°C for wafer splitting.

Fig. 6 is a block diagram of another exemplary embodiment of a semiconductor structure 600. The structure 600 includes a graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 604 grown on a silicon substrate 602, where the Ge concentration x is increased from zero to 1. Then a relaxed pure Ge layer 606 and a III-V material layer 608, such as a GaAs layer, are epitaxially grown on the Ge layer. Hydrogen ions are implanted into the GaAs layer 608 with a selected depth by adjusting implantation energy, forming a buried hydrogen-rich layer 610. The wafer is cleaned and bonded to an oxidized handle wafer 612. An anneal treatment splits the bonded pair at the hydrogen-rich layer 610. As a result, the upper portion of the GaAs layer 608 remains on the oxidized handle wafer, forming a GaAs-on-insulator substrate.

Fig. 7. is a block diagram of yet another exemplary embodiment of a

semiconductor structure 700. A graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 704 is grown on a silicon substrate 702, where the Ge concentration x is increased from zero to a selected value y, where y is less than 0.2. A second relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer 706 is deposited, where z is between 0.2 to 0.25. Hydrogen ions are implanted into the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 5 704 with a selected depth, forming a buried hydrogen-rich layer 708 within layer 704. The wafer is cleaned and bonded to an oxidized handle wafer 710. An anneal treatment at 500~600C° splits the bonded pair at the hydrogen-rich layer 708.

As a result, the upper portion of the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 704 and the relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer 706 remains on the oxidized handle wafer 710. The remaining 10 graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 704 is then selectively etched by either KOH or TMAH. KOH and TMAH etch  $\text{Si}_{1-x}\text{Ge}_x$  fast when x is less 0.2, but becomes very slow when x is larger than 0.2. Thus, the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 704 can be etched 15 selectively, leaving the relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer 706 on the insulating substrate 710 and forming a relaxed SGOI substrate. In this process, the thickness of the relaxed  $\text{Si}_{1-z}\text{Ge}_z$  film 706 on the final SGOI structure is defined by film growth, which is desired in some applications.

Fig. 8 is a block diagram of yet another exemplary embodiment of a semiconductor structure 800. A graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 804 is grown on a silicon substrate 802, where the Ge concentration x is increased from zero to a selected value y 20 between 0 and 1. A second relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer 806 is deposited, followed by a strained  $\text{Si}_{1-z}\text{Ge}_z$  layer 808 and another relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer 810. The thickness of layers 806, 808, and 810, and the value z are chosen such that the  $\text{Si}_{1-z}\text{Ge}_z$  layer 808 is under equilibrium strain state while the  $\text{Si}_{1-y}\text{Ge}_y$  layers 806 and 810 remain relaxed. In one option, hydrogen ions may be introduced into the strained  $\text{Si}_{1-z}\text{Ge}_z$  layer 808, 25 forming a hydrogen-rich layer 812. The wafer is cleaned and bonded to an oxidized handle wafer 814. The bonded pair is then separated along the strained  $\text{Si}_{1-z}\text{Ge}_z$  layer 808.

Since the strain makes the layer weaker, the crack propagates along this layer during separation. The separation can be accomplished by a variety of techniques, for 30 example using a mechanical force or an anneal treatment at 500~600C° when the hydrogen is also introduced. See, for example, U.S. Pat. Nos. 6,033,974 and 6,184,111, both of which are incorporated herein by reference. As a result, the relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer 810 remains on the oxidized handle wafer, forming a relaxed SGOI substrate. The thickness of layers 806, 808, and 810, and the value z may also be chosen such that there are a good 35 amount of dislocations present in the  $\text{Si}_{1-z}\text{Ge}_z$  layer 808 while the top  $\text{Si}_{1-y}\text{Ge}_y$  layer 810

remains relaxed and having high quality and limited dislocation defects.

These dislocation defects in the  $\text{Si}_{1-z}\text{Ge}_z$  layer 808 can then act as hydrogen trap centers during the subsequent step of introducing ions. The hydrogen ions may be introduced by various ways, such as ion implantation or ion diffusion or drift by means 5 of electrolytic charging. The value of z may be chosen in such a way that the remaining  $\text{Si}_{1-z}\text{Ge}_z$  layer 808 can be etched selectively by KOH or TMAH. The layers 806 and 810 may also be some other materials, for example pure Ge, or some III-V materials, under the condition that the Ge concentration x in the graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer 804 is increased from zero to 1.

10 After all the semiconductor-on-insulator substrate obtained by the approaches described above, various device layers can be further grown on the top. Before the regrowth, CMP maybe used to polish the surface.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the 15 form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1        1. A process of forming a semiconductor structure with a relaxed  $\text{Si}_{1-y}\text{Ge}_y$ ,  
2    layer, comprising:

3        depositing a graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer on a first substrate, wherein said Ge  
4    concentration x is increased from zero to a value y;  
5        depositing a relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer;  
6        introducing ions into said relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer to define a first heterostructure;  
7        bonding said first heterostructure to a second substrate to define a second  
8    heterostructure;

9        splitting said second heterostructure in the region of the introduced ions,  
10   wherein a top portion of said relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer remains on said second substrate.

1        2. The process of claim 1 further comprising forming at least one device layer  
2    or a plurality of integrated circuit devices, after said step of depositing said relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer.

1        3. The process of claim 2, wherein said at least one device layer comprises at  
2    least one of strained Si, strained  $\text{Si}_{1-w}\text{Ge}_w$  with  $w \neq y$ , strained Ge, GaAs, AlAs, ZnSe  
3    and InGaP.

1        4. The process of claim 1 further comprising forming an insulating layer before  
2    said step of introducing ions.

1        5. The process of claim 1 further comprising planarizing said relaxed  $\text{Si}_{1-y}\text{Ge}_y$ ,  
2    layer, before said step of introducing ions.

1        6. The process of claim 1, wherein said ions comprise hydrogen  $\text{H}^+$  ions or  $\text{H}_2^+$   
2    ions.

1        7. The process of claim 1 further comprising planarizing said relaxed  $\text{Si}_{1-y}\text{Ge}_y$ ,  
2    layer, after said step of introducing ions.

1        8. The process of claim 1 further comprising cleaning both said first  
2    heterostructure and said second substrate, before said step of bonding.

1        9. The process of claim 1, wherein said second heterostructure is split by  
2    annealing.

1           10. The process of claim 1, wherein said second heterostructure is  
2 split by annealing followed by mechanical force.

1           11. The process of claim 1 further comprising removing the top portion of the  
2 remaining of said relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer, after said step of splitting.

1           12. The process of claim 1 further comprising forming at least one device layer,  
2 or a plurality of integrated circuit devices, after said step of splitting.

1           13. The process of claim 12, wherein said at least one device layer comprises at  
2 least one of relaxed  $\text{Si}_{1-y}\text{Ge}_y$ , strained Si, strained  $\text{Si}_{1-w}\text{Ge}_w$ , strained Ge, GaAs, AlAs,  
3 ZnSe and InGaP.

1           14. The process of claim 1 further comprising re-using the remaining first  
2 heterostructure, after said step of splitting.

1           15. The process of claim 1, wherein said first substrate comprises  
2 monocrystalline silicon.

1           16. A process of forming a semiconductor layer, comprising:

2                 depositing a graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer on a first substrate, said Ge  
3 concentration x being increased from zero to 1;

4                 depositing a relaxed Ge layer;

5                 forming a monocrystalline semiconductor layer including another  
6 material whose lattice constant is approximately close to that of Ge;

7                 introducing ions into said semiconductor layer to define a first  
8 heterostructure;

9                 bonding said first heterostructure to a second substrate to define a  
10 second heterostructure;

11                 splitting said second heterostructure in the region of introduced ions,  
12 wherein a top portion of said semiconductor layer remains on said second substrate.

1           17. The process of claim 16, wherein said semiconductor layer comprises one  
2 of GaAs, AlAs, ZnSe and InGaP.

1        18. The process of claim 16 further comprising forming at least one  
2    device layer or a plurality of integrated circuit devices, after said step of forming said  
3    semiconductor layer.

1        19. The process of claim 16 further comprising forming an insulating layer  
2    before said step of introducing ions.

1        20. The process of claim 16 further comprising planarizing said semiconductor  
2    layer before said step of introducing ions.

1        21. The process of claim 16, wherein said ions comprise hydrogen H<sup>+</sup> ions or  
2    H<sub>2</sub><sup>+</sup> ions.

1        22. The process of claim 16, further comprising the step of planarizing said  
2    semiconductor layer after said step of introducing ions.

1        23. The process of claim 16 further comprising cleaning both said first  
2    heterostructure and said second substrate, before said step of bonding.

1        24. The process of claim 16, wherein said second heterostructure is split by  
2    annealing.

1        25. The process of claim 16, wherein said second heterostructure is split by  
2    annealing and followed by mechanical force.

1        26. The process of claim 16 further comprising removing the top portion of the  
2    remaining of said third semiconductor layer, after said step of splitting.

1        27. The process of claim 16 further comprising forming at least one device  
2    layer or a plurality of integrated circuit devices, after said step of splitting.

1        28. The process of claim 16 further comprising re-using the remaining first  
2    heterostructure, after said step of splitting.

1        29. The process of claim 16, wherein said first substrate comprises  
2    monocrystalline silicon.

1        30. A process of forming a semiconductor structure with a relaxed Si<sub>1-z</sub>Ge<sub>z</sub>  
2    layer, comprising:

3           depositing a graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer on a first substrate, said Ge  
4 concentration x being increased from zero to a selected value y, and y being less than 0.2;

5           depositing a relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer, where z is between 0.2 and 0.25;

6           introducing ions into said graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer to define a first  
7 heterostructure;

8           bonding said first heterostructure to a second substrate to define a  
9 second heterostructure;

10          splitting said second heterostructure in the region of introduced ions,  
11 wherein the upper portion of first graded  $\text{Si}_{1-x}\text{Ge}_x$  layer and said relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer  
12 remains on said second substrate; and

13          selectively etching the remaining portion of said graded  $\text{Si}_{1-x}\text{Ge}_x$  layer,  
14 wherein said relaxed  $\text{Si}_{1-z}\text{Ge}_z$  layer remains on said second substrate.

1           31. The process of claim 30 further comprising forming at least one device  
2 layer or a plurality of integrated circuit devices, after said step of forming said relaxed  
3  $\text{Si}_{1-z}\text{Ge}_z$  layer.

1           32. The process of claim 31, wherein said at least one device layer includes one  
2 or more of strained Si, strained  $\text{Si}_{1-w}\text{Ge}_w$  with  $w \neq z$ , and strained Ge.

1           33. The process of claim 30 further comprising forming an insulating layer  
2 before said step of introducing ions.

1           34. The process of claim 30 further comprising planarizing said relaxed  $\text{Si}_{1-}$   
2  $\text{Ge}_z$  layer before said step of introducing ions.

1           35. The process of claim 30, wherein said ions comprise hydrogen  $\text{H}^+$  ions or  
2  $\text{H}_2^+$  ions.

1           36. The process of claim 30 further comprising planarizing the relaxed  $\text{Si}_{1-z}\text{Ge}_z$   
2 layer after said step of introducing ions.

1           37. The process of claim 30 further comprising cleaning both said first  
2 heterostructure and said second substrate, before said step of bonding.

1           38. The process of claim 30,           wherein said second heterostructure is  
2       split by annealing.

1           39. The process of claim 30 further comprising planarizing said second relaxed  
2        Si<sub>1-z</sub>Ge<sub>z</sub> layer after said step of etching.

1 .40. The process of claim 30 further comprising forming at least one device  
2 layer or a plurality of integrated circuit devices, after said step of etching.

1           41. A process of forming a semiconductor layer, comprising:  
2           depositing a graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer on a first substrate, said Ge  
3           concentration x being increased from zero to a value y;

4 depositing a relaxed Si<sub>1-y</sub>Ge<sub>y</sub> layer;

5 depositing a strained or defect layer;

6 depositing a relaxed layer;

7 introducing ions into said strained or defect layer to define a first  
8 heterostructure;

bonding said first heterostructure to a second substrate to define a second heterostructure; and

11 splitting said second heterostructure in the region of the strained or  
12 defect layer, wherein said relaxed layer remains on said second substrate.

42. The process of claim 41, wherein said strained or defect layer comprises  
either a strained  $\text{Si}_{1-z}\text{Ge}_z$  layer with  $z \neq y$ , or other III-V material.

1           43. The process of claim 41, wherein said relaxed layer or said strained or  
2 defect layer comprises either a relaxed  $\text{Si}_{1-w}\text{Ge}_w$  layer where w is close or equal to y, or,  
3 when y is equal to 1, one of Ge, GaAs, AlAs, ZnSe and InGaP.

1           44. The process of claim 41 further comprising forming at least one device  
2         layer or a plurality of integrated circuit devices, after said step of depositing said  
3         relaxed layer.

1           45. The process of claim 41 further comprising forming an insulating layer  
2 before said step of introducing ions.

1           46. The process of claim 41 further comprising planarizing said relaxed layer  
2 before said step of introducing ions.

1           47. The process of claim 41,           wherein said ions comprise hydrogen H<sup>+</sup>  
2       ions or H<sub>2</sub><sup>+</sup> ions.

1           48. The process of claim 41 further comprising planarizing said relaxed layer  
2 after said step of introducing ions.

1           49. The process of claim 41 further comprising cleaning both said first  
2 heterostructure and said second substrate, before said step of bonding.

1           50. The process of claim 41, wherein said second heterostructure is split by  
2 annealing.

1        51. The process of claim 41 further comprising removing one of any remaining  
2        of said strained or defect layer, and the top portion of said relaxed layer, after said step  
3        of splitting.

1           52. The process of claim 41 further comprising forming at least one device  
2         layer or a plurality of integrated circuit devices, after said step of splitting.

1        53. The process of claim 41 further comprising re-using the remaining first  
2 heterostructure for a subsequent process after planarizing.

1        54. A semiconductor structure comprising:  
2            a first semiconductor substrate;  
3            a second layer of relaxed  $\text{Si}_{1-x}\text{Ge}_x$ , wherein  $x = 0.1$  to  $1$ ; and  
4            a third layer comprising at least one of GaAs, AlAs, ZnSe and InGaP, or  
5            strained  $\text{Si}_{1-y}\text{Ge}_y$  wherein  $y \neq x$ .

1        55. A semiconductor structure comprising:  
2              a first substrate comprising monocrystalline silicon substrate;  
3              a second layer of graded  $\text{Si}_{1-x}\text{Ge}_x$  buffer layer, wherein said Ge concentration x  
4          is increased from zero to a value y;  
5              a third layer of relaxed  $\text{Si}_{1-y}\text{Ge}_y$  ;  
6              a fourth strained or defect layer comprising either a strained  $\text{Si}_{1-z}\text{Ge}_z$  layer with  
7           $z \neq y$ , or other III-V or II-VI material; and  
8              a fifth relaxed layer comprising either a relaxed  $\text{Si}_{1-w}\text{Ge}_w$  layer where w is close  
9          or equal to y, or, when y is equal to 1, at least one of Ge, GaAs, AlAs, ZnSe and InGaP.

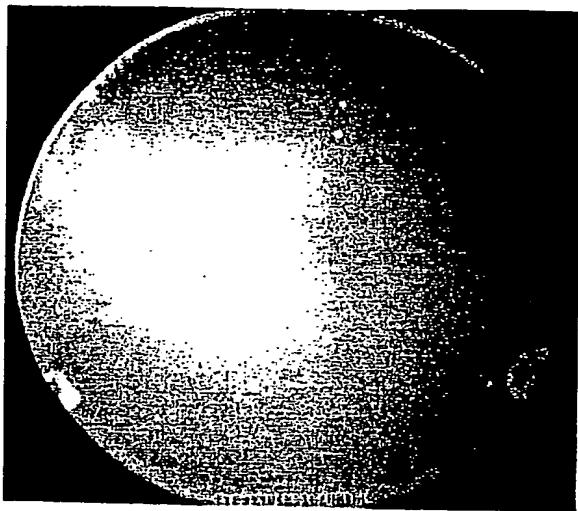


Fig. 2A

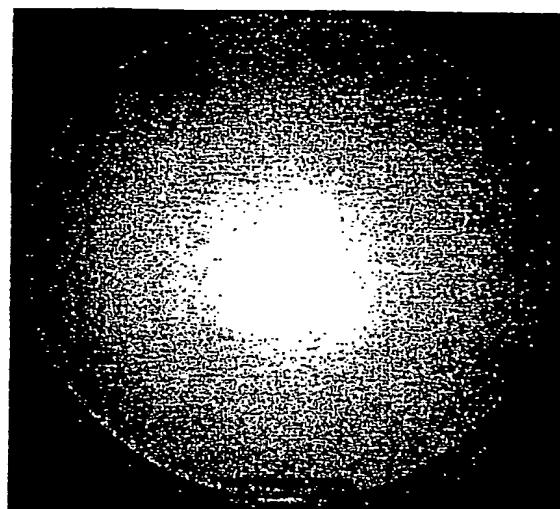


Fig. 2B

Fig. 1A

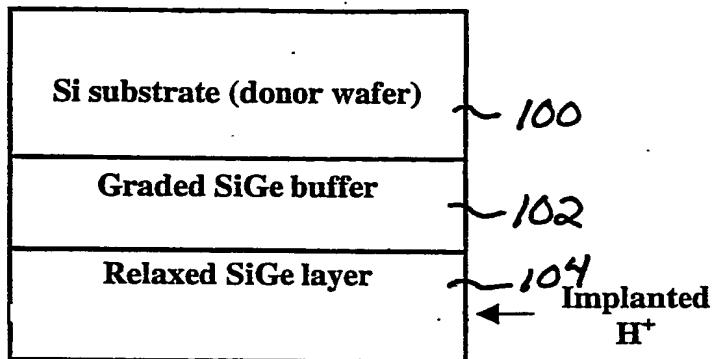


Fig. 1B

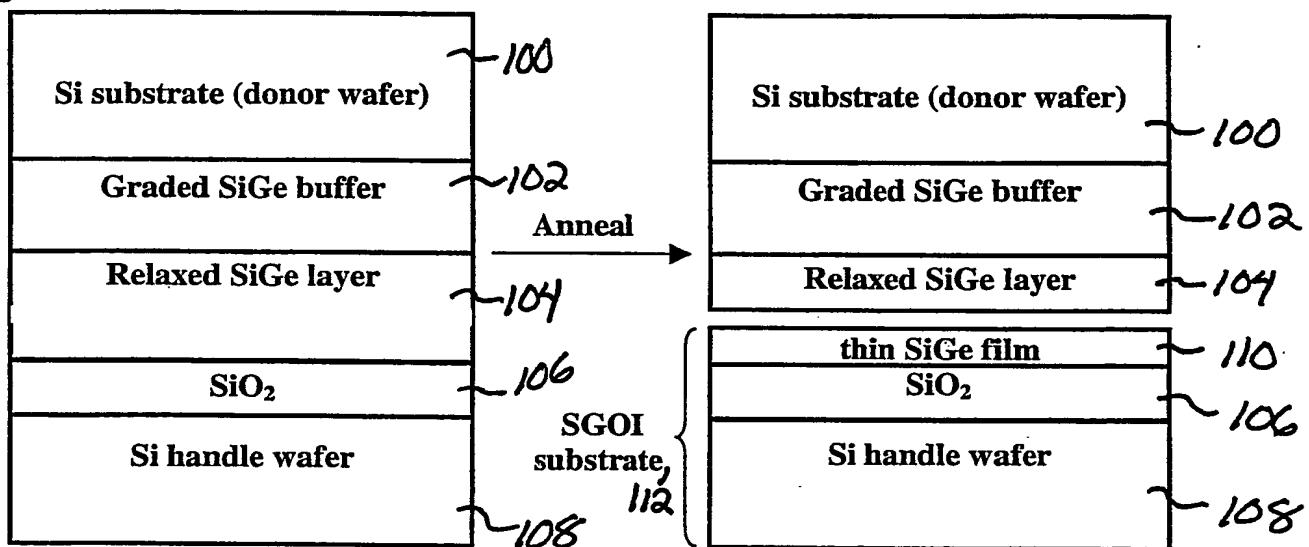


Fig. 1C

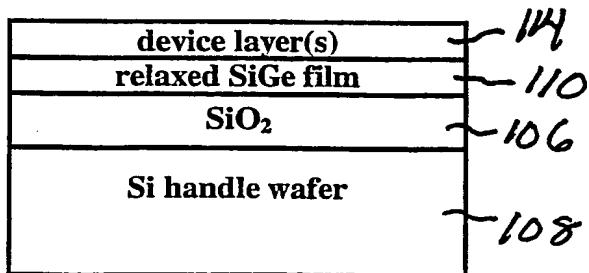
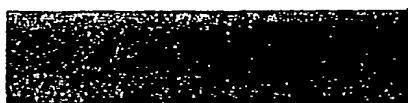


Fig. 3



← splitting surface  
← 25% relaxed SiGe  
(~ 640 nm)  
← BOX (550 nm)



← Si (100)

200 nm

Fig. 4

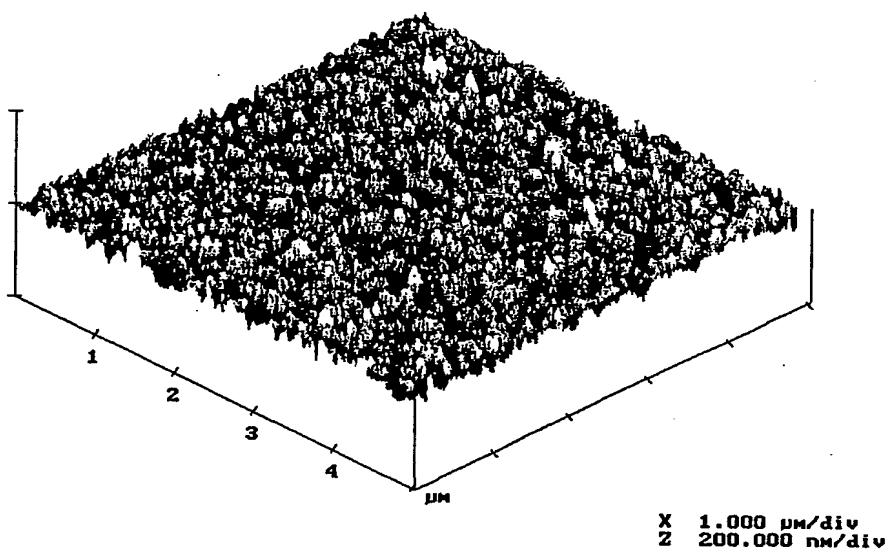


Fig. 5

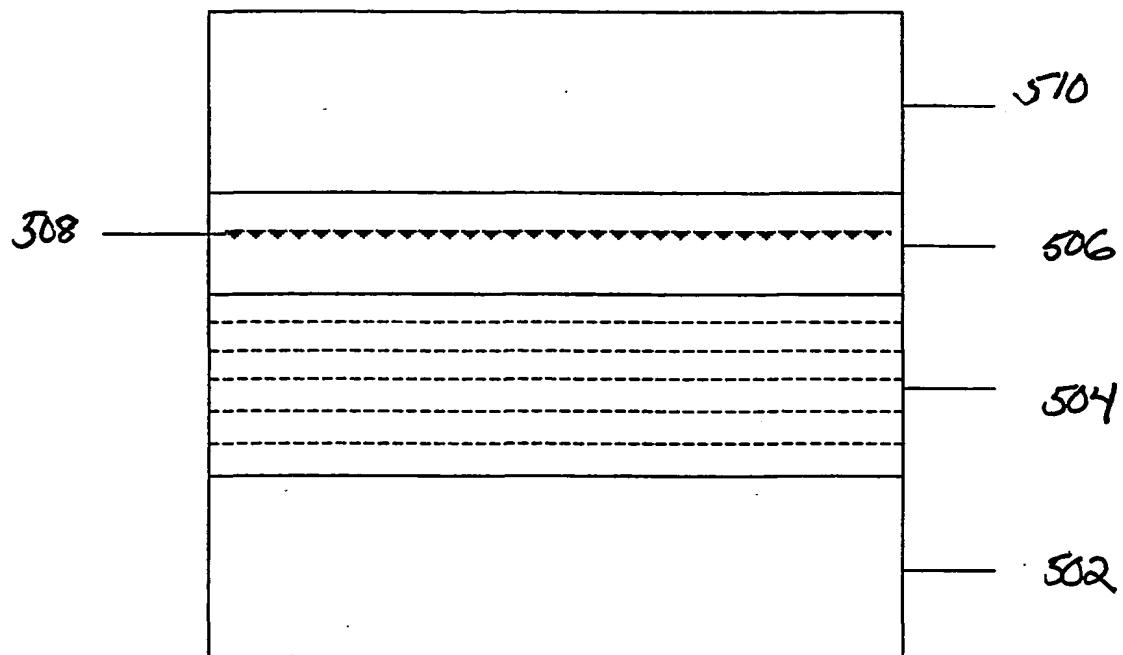


Fig. 6

600  
↓

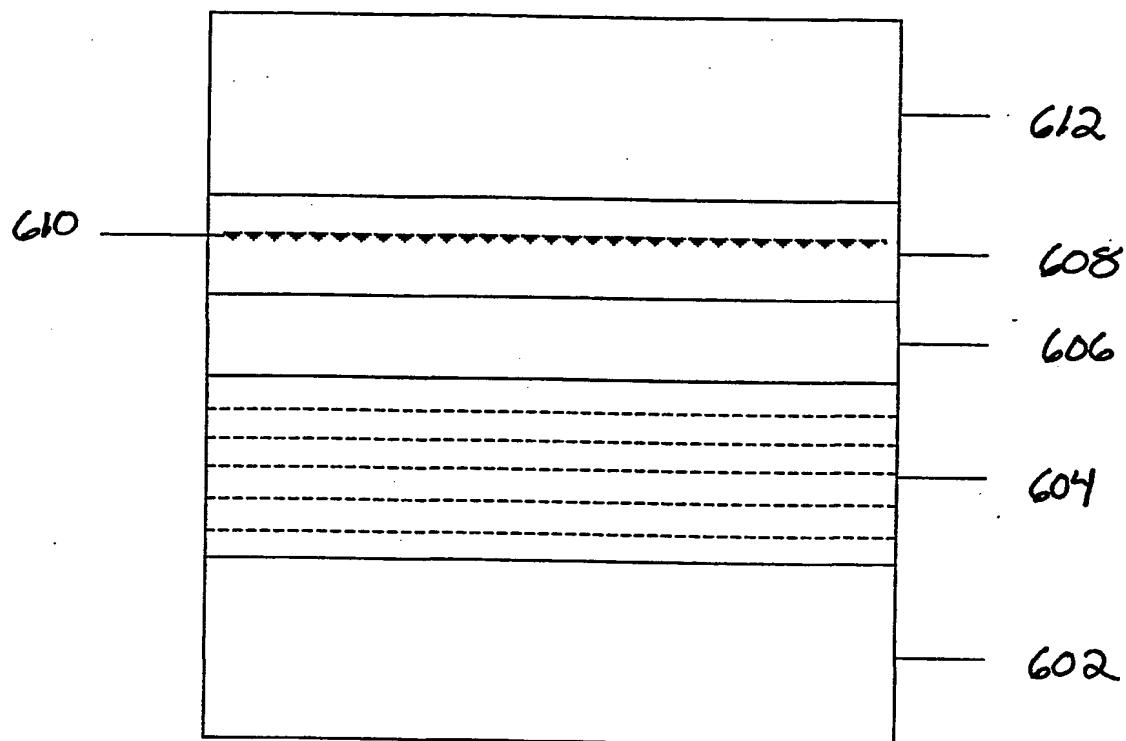


Fig. 7 700

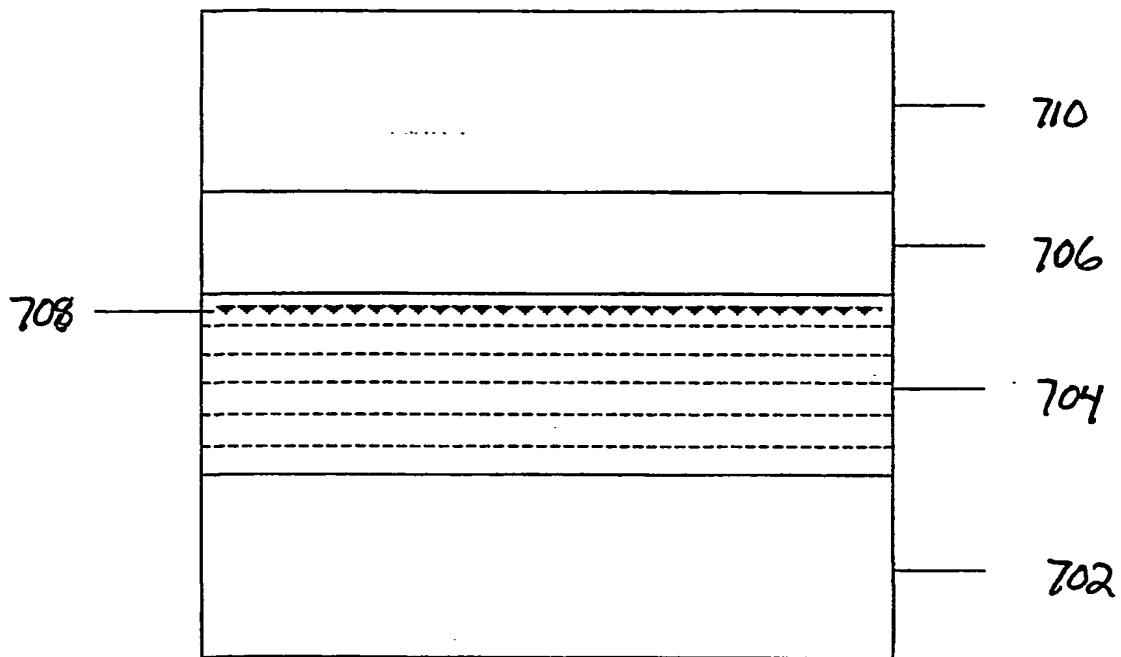
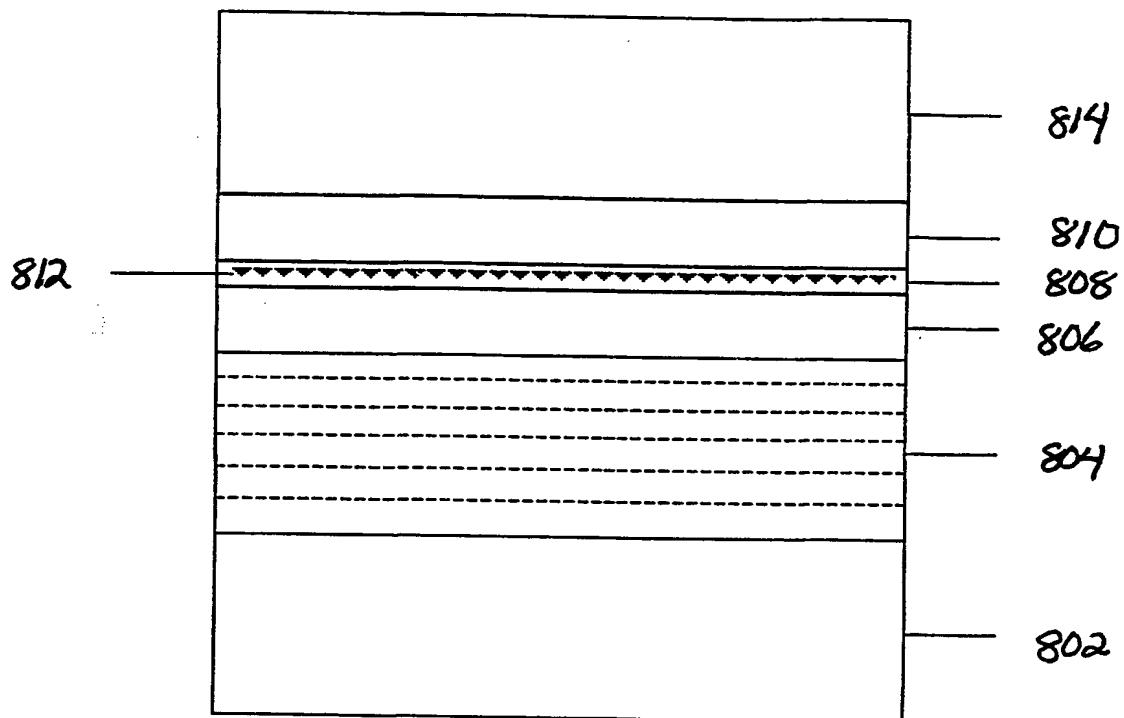


Fig. 8  
800  
↓



(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
21 February 2002 (21.02.2002)

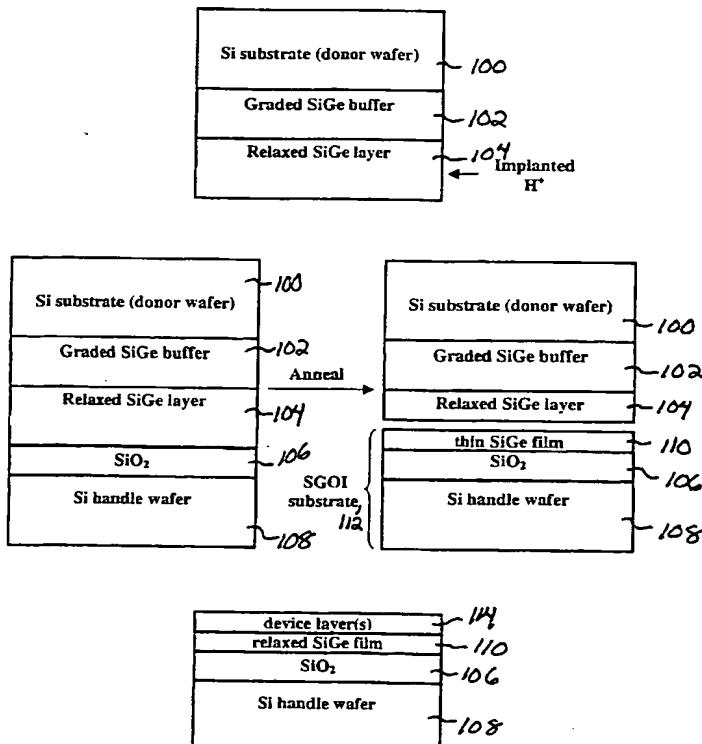
PCT

(10) International Publication Number  
WO 02/015244 A3

- (51) International Patent Classification<sup>7</sup>: H01L 21/205, (74) Agents: CONNORS, Matthew, E. et al.; Samuels, Gauthier & Stevens, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).
- (21) International Application Number: PCT/US01/41680
- (22) International Filing Date: 10 August 2001 (10.08.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
60/225,666 16 August 2000 (16.08.2000) US
- (71) Applicant: CHENG, Zhi-Yuan [US/US]; 14 Seventh Street, Cambridge, MA (US).
- (72) Inventors: FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US). ANTONIADIS, Dimitri, A.; 195 Beethoven Avenue, Newton, MA 02168 (US). HOYT, Judy, L.; 32 Springfield Street, Belmont, MA 02478 (US).
- (81) Designated States (national): CA, JP, KR.
- (84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).
- Published:  
— with international search report
- (88) Date of publication of the international search report:  
31 October 2002

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

## (54) Title: PROCESS FOR PRODUCING SEMICONDUCTOR ARTICLE USING GRADED EXPITAXIAL GROWTH



(57) Abstract: A process for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded  $\text{Si}_{1-x}\text{Ge}_x$  (x increases from 0 to y) is deposited on a first silicon substrate, followed by deposition of a relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer, a thin strained  $\text{Si}_{1-z}\text{Ge}_z$  layer. Hydrogen ions are then introduced into the strained  $\text{Si}_2\text{Ge}_z$  layer. The relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, such that the second relaxed  $\text{Si}_{1-y}\text{Ge}_y$  layer remains on the second substrate. In another exemplary embodiment, a graded  $\text{Si}_{1-x}\text{Ge}_x$  is deposited on a first silicon substrate, where the Ge concentration x is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth. The relaxed GaAs layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the hydrogen ion rich layer, such that the upper portion of relaxed GaAs layer remains on the second substrate.

WO 02/015244 A3

## INTERNATIONAL SEARCH REPORT

International Application No  
PCT/US 01/41680

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 H01L21/205 H01L21/331

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 759 898 A (PITNER PHILIP MICHAEL ET AL) 2 June 1998 (1998-06-02) cited in the application abstract ---	1-53
X	US 5 906 951 A (CHU JACK OON ET AL) 25 May 1999 (1999-05-25) cited in the application figure 1 ---	54,55
X	US 5 442 205 A (BRASEN DANIEL ET AL) 15 August 1995 (1995-08-15) abstract -----	54,55

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

## \* Special categories of cited documents :

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
- \*E\* earlier document but published on or after the international filing date
- \*L\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

- \*T\* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- \*X\* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- \*Y\* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- \*&\* document member of the same patent family

Date of the actual completion of the international search

9 July 2002

Date of mailing of the international search report

17/07/2002

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl.  
Fax: (+31-70) 340-3016

Authorized officer

Le Meur, M-A

## INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 01/41680

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5759898	A	02-06-1998	US EP JP JP	5461243 A 0651439 A2 2694120 B2 7169926 A	24-10-1995 03-05-1995 24-12-1997 04-07-1995
US 5906951	A	25-05-1999	JP JP TW US	2908787 B2 10308503 A 388969 B 6059895 A	21-06-1999 17-11-1998 01-05-2000 09-05-2000
US 5442205	A	15-08-1995	US EP JP JP	5221413 A 0514018 A2 2792785 B2 6252046 A	22-06-1993 19-11-1992 03-09-1998 09-09-1994

THIS PAGE BLANK (USPTO)